Using The HI7188 Serial Interface

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Introduction

The HI7188 Serial Interface is designed to be compatible with many industry standard synchronous transfer formats including the Motorola 6805/11 series SPI and Intel 8051 SSR protocols. The advantage of HI7188 Serial Interface is its flexibility. However, flexibility has its price - complexity. The complexity of the HI7188 Serial Interface may lead to confusion for first time users. This Application Note discusses general serial interface issues associated with the HI7188. It is assumed the reader has read the HI7188 data sheet and understands the basic operational details of the device.

The HI7188 allows read/write access to the Control Register (CR), the Channel Configuration Registers (CCR#1, CCR#2) as well as the Calibration RAMs. The Data RAM, which contains the conversion results, is read only.

Serial Interface Functionality

Communication with the HI7188 occurs in what are called communication cycles and each communication cycle contains two phases. Figure 1 shows that the first phase of every communication cycle is the writing of an instruction byte. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte. The instruction byte provides the HI7188 Serial Interface with information regarding the data transfer in phase 2 of the communication cycle. The remaining SCLK edges are used for phase 2 of the communication cycle. Phase 2 is the actual data transfer between the HI7188 and the processor.

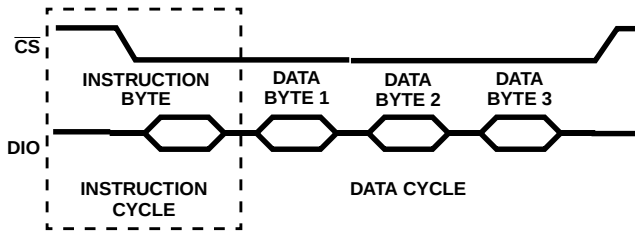

FIGURE 1. 3 BYTE COMMUNICATION CYCLE

Phase 2 of the communication cycle is determined by the instruction byte written. For Registers (Control, CCR#2 and CCR#1), phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by two IR bits. For RAMs (Data RAM and Calibration RAMs), phase 2 of the communication cycle is a transfer of all data bytes for each active logical channel as determined by the N bits of the Control Register (CR<7:5>) in addition to the instruction byte It is important to note that the instruction byte is interpreted differently for register accesses than for RAM accesses.

Having programmability over the number of bytes to transfer suggests there are several ways to read or write a multi-byte register. For example, a 3 byte data transfer can be completed in one communication cycle by writing the instruction byte to transfer 3 bytes of data. Or, the same 3 byte data transfer can be spread over three communication cycles by writing the instruction byte to transfer 1 byte of data with three separate communication cycles. Finally, this same 3 byte data transfer can be accomplished over two communication cycles as well by writing the instruction byte for a 2 byte transfer followed by another single byte communication cycle or vice versa! Flexibility is increased even further since the instruction byte contains the starting byte address of the register from which data is transferred.

Normally using one communication cycle in a multi-byte transfer is the preferred method. However, single byte communication cycles are useful to reduce CPU overhead when a register access requires only one byte of data to be transferred. For example, the HI7188 can be put into the sleep mode by a single byte write to the Control Register (CR).

The user does not have multi-byte control when accessing the RAMs of the HI7188. In fact, when accessing the HI7188 RAMs, all bytes for each active logical channel will be transferred. The word order is first logical channel to last logical channel. Most significant byte first or least significant byte first format is programmable for RAM access as well as register access.

It is important to note that the instruction byte written during phase 1 of the communication cycle describes the number of bytes to be transferred during phase 2. This means that the number of bytes transferred as described in the instruction byte does not include the instruction byte write of phase 1. For example, see Figure 1, which shows a three byte communication cycle.

The processor must maintain synchronism with the HI7188, or the internal communication controller will not be able to recognize further instructions. For example, if the processor sends an instruction byte for a two byte read and then pulses SCLK for a 3 byte read (24 falling edges), communication synchronization is lost. This is because the first 16 SCLK falling edges after the instruction byte write caused data to be read out of the HI7188. But according to the instruction byte, that was the end of the communication cycle. So the HI7188 interpreted the last 8 SCLK rising edges as the next instruction byte. This would cause communication problems as the HI7188 believes it is in the middle of another communication cycle; but the processor believes a communication cycle has just ended. The way to recover from this type of error is to pulse the $\overline{\text{RSTI/O}}$ pin low, resetting the HI7188 I/O controller. Pulsing the $\overline{\text{RSTI/O}}$ pin low will not alter the contents of any I/O accessible memory elements. It forces the

HI7188 serial interface into a state in which the next 8 SCLK cycles are interpreted as phase 1 of the communication cycle. That is, after $\overline{RSTI/O}$ goes back high, the user can begin a new communication cycle.

The instruction byte specification is as follows:

MSB	6	5	4	3	2	1	LSB
$\overline{R}$/W	NB1	NB0	RB	A3	A2	A1	A0

$\overline{R}$/W - Bit 7 of the instruction byte determines whether phase 2 of the communication cycle will be a read or write operation. If $\overline{R}$/W is logic 1, a write transfer will occur in phase 2 of the communication cycle. If $\overline{R}$/W is logic 0, a read transfer will occur in phase 2 of the communication cycle.

NB1, NB0 - Bits 6 and 5 of the instruction byte determine the number of bytes that will be transferred during phase 2 of the communication cycle, If a register is selected for I/O access. If a RAM is selected for I/O access, these bits are don't care. Any number of bytes from 1 to 4 is allowed. See the HI7188 data sheet for specific bit decodes.

RB - Bit 4 is used to determine the byte order when accessing a RAM address. When accessing a RAM address, if RB=1, the data format is most significant byte first to least significant byte. When accessing a RAM address, if RB=0, the data format is least significant byte first to most significant byte. When accessing a register address, this bit is a don't care.

A3, A2, A1, A0 - Bits 3 and 2 (A3 and A2) of the instruction byte determine which of the three internal registers will be accessed or if both bits are set (11b), that a RAM access is active. For register addresses, bits 1 and 0 (A1 and A0) determine which byte of that register will be accessed first. For RAM access (A3=1,A2=1), bits 1 and 0 (A1 and A0) determine which RAM is the source or destination. See the HI7188 data sheet for specific address requirements.

In addition to understanding the communication cycle concept it is important to note that the three least significant bits of the CR have a large impact on the serial interface. The least significant bit (CR<0>) determines whether one line or two line protocol is used. For one line protocol the SDIO pin is used for data input and output, while for 2 line protocol the SDIO pin is used for data input and the SDO pin is used for data output. The CR<2> and CR<1> bits are the Byte Direction (BD) and $\overline{MSB}$ bits respectively. The BD bit specifies whether data bytes will be accessed in ascending or descending order (register addresses only). The $\overline{MSB}$ bit specifies if each byte will be accessed MSB first or LSB first. This bit applies for both register and RAM addresses. Together, these bits allow the user to access data in MSB to LSB format or LSB to MSB format.

Practical Examples

Below are useful examples of write and read communication cycles which illustrate the serial interface functionality. Please refer to the datasheet for detailed register descriptions.

Example 1: 4 Byte Write Operation of the CCR#2, MSB to LSB format

The 4-Byte Channel Configuration Register (CCR#2) can be written to using one multi-byte communication cycle rather than four single byte communication cycles. For this example the data will be transferred from MSB to LSB format so the CR must be configured for descending byte direction and MSB first bit positioning. Therefore, the BD and $\overline{MSB}$ bits are programmed to logic zero. To achieve this write operation the user performs the following:

Instruction Cycle

The system microprocessor sends an instruction byte comprised of 1110 1011 (EB_{hex}) to the Instruction Register (IR). Please note the RB bit IR<4> is a don't care since this bit only pertains to a RAM I/O access. The following is a breakdown of this instruction byte.

INSTRUCTION BYTE

MSB	6	5	4	3	2	1	LSB
$\overline{R}$/W	NB1	NB0	RB	A3	A2	A1	A0
1	1	1	X	1	0	1	1

This instruction byte provides the following information about the pending data cycle:

- Write operation
- 4 bytes of data
- The register is CCR#2, starting byte 3.

Data Cycle

The HI7188 serial interface controller receives the 4 bytes from the microprocessor, registering each bit on the rising edge of the SCLK. The data is written to the CCR#2 starting with byte 3 and continuing with bytes 2,1 and 0.

Example 2: Read of Data RAM, MSB to LSB Format

The powerful HI7188 serial interface performs all RAM I/O transfers in a "Burst" mode. The Burst transfers are special instructions that perform a continuous data transfer for all bits of the RAM. The number of bytes transferred is set based on the number of active logical channels. For this example the data will be transferred from MSB to LSB format so the CR must be configured for descending byte direction and MSB first bit positioning. Therefore, the BD and $\overline{MSB}$ bits are programmed to logic zero. To achieve a "Burst" read of the Data RAM the user performs the following:

Instruction Cycle

The system microprocessor sends an instruction byte comprised of 0001 1100 ($1C_{hex}$) to the instruction register (IR). Please note the NB1, NB0 bits are a don't care since these bits do not pertain to a RAM access. The following is a breakdown of this instruction byte.

INSTRUCTION BYTE

MSB	6	5	4	3	2	1	LSB
$\overline{R}$/W	NB1	NB0	RB	A3	A2	A1	A0
0	X	X	1	1	1	0	0

This instruction byte provides the following information about the pending data cycle:

- Read operation
- 16 bytes of data (Assuming 8 logical channels are active)
- The source is the Data RAM, most significant byte first

Data Cycle

The HI7188 serial interface controller sends 16 data bytes starting with the most significant bit (MSB) and continuing to the least significant bit (LSB) of the Data RAM. Each bit is driven out on the falling edge of SCLK. The first byte transferred is the most significant byte of logical channel 1 followed by the least significant byte of logical channel 1. This pattern of most significant byte followed by least significant byte will be repeated for logical channels 2,3,4,5,6,7, and 8.

Example 3: Read of the Positive Full Scale Calibration RAM, LSB to MSB Format

The Positive Full Scale Calibration RAM can be read using one RAM burst read operation. Assuming 8 logical channels are active, 24 data bytes will be transferred. The data represents 3 bytes for each of the 8 logical channels. For this example the data will be transferred from LSB to MSB format so the CR must be configured for ascending byte direction and LSB first bit positioning. Therefore, the BD and $\overline{MSB}$ bits are programmed to logic one. To achieve this read operation the user performs the following:

Instruction Cycle

The system microprocessor sends an instruction byte comprised of 0000 1110($0E_{hex}$) to the instruction register (IR). Please note the NB1, NB0 bits are a don't care since these bits do not pertain to a burst RAM I/O access. The following is a breakdown of this instruction byte.

INSTRUCTION BYTE

MSB	6	5	4	3	2	1	LSB
$\overline{R}$/W	NB1	NB0	RB	A3	A2	A1	A0
0	X	X	0	1	1	1	0

This instruction byte provides the following information about the pending data cycle:

- Read operation
- 24 Bytes of data (3 bytes for 8 channels)
- The source is the Positive Full Scale Calibration RAM, least significant byte first.

Data Cycle

The HI7188 serial interface controller sends 24 data bytes starting with the least significant bit (LSB) and continuing to the most significant bit (MSB) of the Positive Full Scale Calibration RAM. The data bits are driven out on the falling edge of SCLK. The first three bytes transferred pertain to logical channel 1. The first byte transferred is the least significant byte of logical channel 1, followed by the next greater significant byte and finally the most significant byte of logical channel 1. This pattern of least significant byte followed by next greater significant byte and finally the most significant byte will be repeated for logical channels 2,3,4,5,6,7, and 8. The communication cycle is now complete and the entire RAM was read in LSB to MSB format during a single communication cycle.

Example 4: Read of Offset Calibration RAM for 3 Logical Channels, MSB to LSB Format

The Data RAM, Offset Calibration RAM, Positive Full Scale Calibration RAM, and Negative Full Scale Calibration RAM can be fully or partially read in a burst mode depending on the number of active logical channels defined in Control Register (CR). The N2, N1 and N0 bits of the Control Register (CR<7:5>) set the number of active logical channels to be converted. To convert on only three logical channels, N2, N1 and N0 are set to 0,1 and 0 respectively. For this example the data will be transferred in MSB to LSB format so the CR must be configured for MSB first bit positioning ($\overline{MSB}$ = 0). Please note the calibration RAMs are 3 bytes wide for each logical channel. To achieve this read operation the user performs the following:

Instruction Cycle

The system microprocessor sends an instruction byte comprised of 0001 1101($1D_{hex}$). Please note the NB1, NB0 bits are a don't care since these bits do not pertain to a RAM access. The following is a breakdown of this instruction byte.

INSTRUCTION BYTE

MSB	6	5	4	3	2	1	LSB
$\overline{R}$/W	NB1	NB0	RB	A3	A2	A1	A0
0	X	X	1	1	1	0	1

This instruction byte provides the following information about the pending data cycle:

- Read operation
- 9 Bytes of data (3 bytes for 3 channels)
- The source is the offset calibration RAM, most significant byte first.

Data Cycle

The HI7188 serial interface controller sends 9 data bytes starting with the most significant bit (MSB) and continuing to the least significant bit (LSB) of the first 9 bytes of the 24 byte Offset Calibration RAM. The data bits are driven out on the falling edge of SCLK. The first three bytes transferred pertain to logical channel 1. The first byte transferred is the most significant byte of logical channel 1, followed by the next lesser significant byte and finally the least significant byte of logical channel 1. This pattern of most significant byte followed by next lesser significant byte and finally the least significant byte will be repeated for logical channels 2 and 3. Since only 3 channels are active, the remaining 15 bytes for logical channels 4 through 8 are NOT read. The communication cycle is now complete and the three active channels were read in MSB to LSB format in a single communication cycle.

Example 5: Incorrect I/O of Offset Calibration RAM, MSB to LSB Format

The user must be careful when controlling the data transfer format in regards to the byte order. The Control Register $\overline{MSB}$ bit must be consistent with the instruction byte RB bit to prevent erroneous results.

The following is an example of an incorrect transfer. For this example, assume the Control Register is set for three logical channels and the $\overline{MSB}$ bit is logic zero. Therefore, 9 bytes of data will be read (3 bytes for 3 channels) from the Offset Calibration RAM.

Instruction Cycle

The system microprocessor sends an instruction byte comprised of 0000 1101($0D_{hex}$). The following is a breakdown of this instruction byte.

INSTRUCTION BYTE

MSB	6	5	4	3	2	1	LSB
$\overline{R}$/W	NB1	NB0	RB	A3	A2	A1	A0
0	X	X	0	1	1	0	1

This instruction byte provides the following information about the pending data cycle:

- Read operation
- 9 bytes of data (3 bytes for 3 channels)
- The source is the Offset Calibration RAM
- The byte order is least significant to most significant

Data Cycle

The instruction byte is the source of the error because the RB bit is logic zero causing the byte order to start at the least significant byte and end at the most significant byte. This is inconsistent with the bit order defined in the Control Register. With this inconsistent configuration the following transfer would occur.

The data of the least significant byte of the first logical channel is driven out of the HI7188 on the falling edges of SCLK in most significant to least significant bit order. After this byte is transferred the HI7188 drives out the next greater significant byte of the first channel followed by the most significant byte for that channel, each byte in MSB to LSB bit order. This sequence of driving out three data bytes repeats for the second logical and third logical channels. The communication cycle is now complete. For each of the three words (logical channels) read, the data output is as follows: d<7:0>,d<15:8>,d<23:16>. Note that each 3 byte word is NOT in MSB to LSB or LSB to MSB format.

Serial Interface Quick Reference

For a quick I/O reference please refer to the table below.

I/O TRANSFER DESCRIPTION

I/O TRANSFER DESCRIPTION	CR <2:1>	IR (HEX)
Control Register write, 16-Bit, MSB to LSB	00	A1
Control Register write, 16-Bit, LSB to MSB	11	A0
Control Register read, 16-Bit, MSB to LSB	00	21
Control Register read, 16-Bit, LSB to MSB	11	20
CCR#2 Register write, 32-Bit, MSB to LSB	00	EB
CCR#2 Register write, 32-Bit, LSB to MSB	11	E8
CCR#2 Register read, 32-Bit, MSB to LSB	00	6B
CCR#2 Register read, 32-Bit, LSB to MSB	11	68
CCR#1 Register write, 32-Bit, MSB to LSB	00	E7
CCR#1 Register write, 32-Bit, LSB to MSB	11	E4
CCR#1 Register read, 32-Bit, MSB to LSB	00	67
CCR#1 Register read, 32-Bit, LSB to MSB	11	64
Data RAM burst read, MSB to LSB	00	1C
Data RAM burst read, LSB to MSB	11	0C
Offset Calibration RAM write, MSB to LSB	00	9D
Offset Calibration RAM write, LSB to MSB	11	8D
Offset Calibration RAM read, MSB to LSB	00	1D
Offset Calibration RAM read, LSB to MSB	11	0D
Positive Full Scale Calibration RAM write, MSB to LSB	00	9E
Positive Full Scale Calibration RAM write, LSB to MSB	11	8E
Positive Full Scale Calibration RAM read, MSB to LSB	00	1E
Positive Full Scale Calibration RAM read, LSB to MSB	11	0E
Positive Full Scale Calibration RAM write, MSB to LSB	00	9F
Negative Full Scale Calibration RAM write, LSB to MSB	11	8F
Negative Full Scale Calibration RAM read, MSB to LSB	00	1F
Negative Full Scale Calibration RAM read, LSB to MSB	11	0F

Further Clarifications

1. When changing the I/O configuration, which defaults to single data line in MSB to LSB bit order, the user must be aware that the configuration changes IMMEDIATELY after completing the write of that CR byte. This may occur in the middle of a communication cycle, depending on how the user writes the IR. It is recommended that the least significant byte of the CR be written last when reconfiguring the serial Interface of the HI7188. Another method would be to use a single byte communication cycle when reconfiguring the serial interface.
2. It is important to realize that if a four byte transfer is requested the HI7188 requires that four bytes be transferred regardless of the number of bytes in the register. That is, if a 2 byte register is being accessed but a four byte transfer is requested, four bytes must be transferred. The first byte accessed will be transferred twice.
3. When the user performs an I/O access of the Calibration RAMs the modulator and digital filter are reset and placed in standby until the I/O is completed. After the I/O access is completed conversions automatically restart.

In review, each HI7188 Register can be accessed on a per byte basis or via multiple byte transfers depending on the instruction byte. Each RAM requires only one instruction byte to transfer the entire content of the RAM. Each communication cycle can be most significant bit to least significant bit order or vice versa depending on the configuration of the BD and $\overline{\text{MSB}}$ bits in the CR and the instruction byte. In addition, the HI7188 can be configured for either one line or two line protocol.

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